

VNN3NV04P-E VNS3NV04P-E

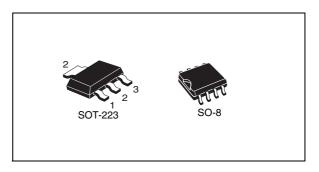
OMNIFET II fully autoprotected Power MOSFET

Datasheet - production data

Features

Туре	R _{DS(on)}	I _{lim}	V _{clamp}
VNN3NV04P-E VNS3NV04P-E	120 mΩ	3.5 A	40 V

- Linear current limitation
- Thermal shutdown
- Short circuit protection
- Integrated clamp
- Low current drawn from input pin
- Diagnostic feedback through input pin
- ESD protection
- Direct access to the gate of the Power MOSFET (analog driving)
- Compatible with standard Power MOSFET in compliance with the 2002/95/EC European directive



Description

The VNN3NV04P-E, VNS3NV04P-E, are monolithic devices designed in STMicroelectronics® VIPower® M0-3 Technology, intended for replacement of standard Power MOSFETs from DC up to 50 kHz applications. Built in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments.

Fault feedback can be detected by monitoring the voltage at the input pin.

Table 1. Device summary

Package	Orde	er codes
rackage	Tube	Tape and reel
SOT-223	_	VNN3NV04PTR-E
SO-8	VNS3NV04P-E	VNS3NV04PTR-E

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1 Block diagram and pin description

Figure 1. Block diagram

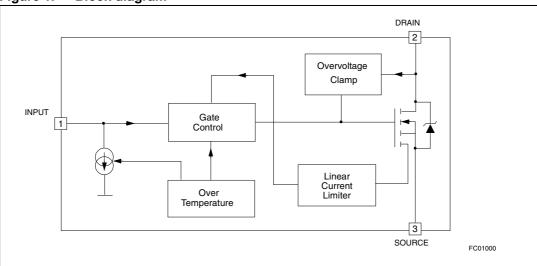
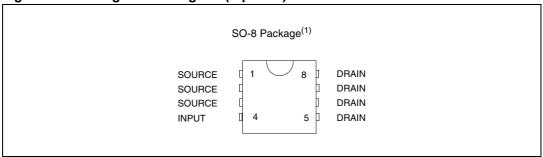


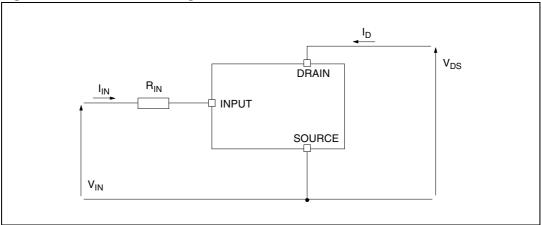
Figure 2. Configuration diagram (top view)



1. For the pins configuration related to SOT-223 see outlines at page 1.

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Sumbal	Parameter	Value		Unit
Symbol	Farameter	SOT-223	SO-8	Offic
V _{DS}	Drain-source voltage (V _{IN} = 0 V)	Internally	clamped	V
V _{IN}	Input voltage	Internally	clamped	V
I _{IN}	Input current	+/-	20	mA
R _{IN MIN}	Minimum input series impedance	22	20	Ω
I _D	Drain current Internally limited		Α	
I _R	Reverse DC output current -5.5		Α	
V _{ESD1}	Electrostatic discharge (R = 1.5 KΩ, C = 100 pF) 4000		V	
V _{ESD2}	Electrostatic discharge on output pin only $(R = 330 \ \Omega, \ C = 150 \ pF)$		V	
P _{tot}	Total dissipation at T _c = 25 °C 7 8.3		8.3	W
T _j	Operating junction temperature Internally limited		°C	
T _c	Case operating temperature Internally limited		y limited	°C
T _{stg}	Storage temperature	-55 to	150	°C

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Val	Unit		
Symbol	r al allietei	SOT-223	SO-8	Oilit	
R _{thj-case}	Thermal resistance junction-case max	18		°C/W	
R _{thj-lead}	Thermal resistance junction-lead max		15	°C/W	
R _{thj-amb}	Thermal resistance junction-ambient max	70 ⁽¹⁾	65 ⁽¹⁾	°C/W	

When mounted on a standard single-sided FR4 board with 50 mm² of Cu (at least 35 mm thick) connected to all DRAIN pins.

2.3 Electrical characteristics

-40°C < T_i < 150°C, unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min	Тур	Max	Unit	
Off	Off						
V _{CLAMP}	Drain-source clamp voltage	V _{IN} = 0 V; I _D = 1.5 A	40	45	55	V	
V _{CLTH}	Drain-source clamp threshold voltage	V _{IN} = 0 V; I _D = 2 mA	36			V	
V _{INTH}	Input threshold voltage	$V_{DS} = V_{IN}$; $I_D = 1 \text{ mA}$	0.5		2.5	V	
I _{ISS}	Supply current from input pin	V _{DS} = 0 V; V _{IN} = 5 V		100	150	μΑ	
V	Input-source clamp voltage	I _{IN} = 1 mA	6	6.8	8	V	
V _{INCL}	input-source clamp voltage	I _{IN} = -1 mA	-1.0		-0.3	V	
1	Zero input voltage drain current (V _{IN} = 0 V)	$V_{DS} = 13 \text{ V}; V_{IN} = 0 \text{ V}; T_j = 25^{\circ}\text{C}$			30	μΑ	
I _{DSS}		V _{DS} = 25 V; V _{IN} = 0 V			75	μΑ	
On							
Б	Static drain-source on	$V_{IN} = 5 \text{ V}; I_D = 1.5 \text{ A}; T_j = 25^{\circ}\text{C}$			120	mΩ	
R _{DS(on)}	resistance	V _{IN} = 5 V; I _D = 1.5 A			240	mΩ	
Dynamic (T _j =25 °C, unless otherwise sp	ecified)					
g _{fs} ⁽¹⁾	Forward transconductance	V _{DD} = 13 V; I _D = 1.5 A		5.0		S	
C _{OSS}	Output capacitance	V _{DS} = 13 V; f = 1 MHz; V _{IN} = 0 V		150		pF	
Switching	(T _j = 25°C, unless otherwise s	specified)					
t _{d(on)}	Turn-on delay time			90	300	ns	
t _r	Rise time	V _{DD} = 15 V; I _D = 1.5 A; V _{gen} = 5 V;		250	750	ns	
t _{d(off)}	Turn-off delay time	$R_{gen} = R_{IN MIN} = 220 \Omega \text{ (see Figure 4)}$		450	1350	ns	
t _f	Fall time			250	750	ns	

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
t _{d(on)}	Turn-on delay time			0.45	1.35	μs
t _r	Rise time	V _{DD} = 15 V; I _D = 1.5 A; V _{qen} = 5 V;		2.5	7.5	μs
t _{d(off)}	Turn-off delay time	$R_{gen} = 2.2 \text{ K}\Omega \text{ (see } Figure 4\text{)}$		3.3	10.0	μs
t _f	Fall time			2.0	6.0	μs
(dl/dt) _{on}	Turn-on current slope	$V_{DD} = 15 \text{ V}; I_{D} = 1.5 \text{ A}; V_{gen} = 5 \text{ V};$ $R_{gen} = R_{IN \text{ MIN}} = 220 \Omega$		4.7		A/µs
Qi	Total input charge	V_{DD} = 12 V; I_{D} = 1.5 A; V_{IN} = 5 V; I_{gen} = 2.13 mA (see <i>Figure 7</i>)		8.5		nC
Source dra	ain diode (T _j =25°C, unless oth	nerwise specified)				
V _{SD} ⁽¹⁾	Forward on voltage	I _{SD} = 1.5 A; V _{IN} = 0 V		8.0		V
t _{rr}	Reverse recovery time	I _{SD} = 1.5 A; dl/dt = 12 A/μs;		107		ns
Q _{rr}	Reverse recovery charge	$V_{DD} = 30 \text{ V}; L = 200 \mu\text{H}$		37		μC
I _{RRM}	Reverse recovery current	(see <i>Figure 5</i>)		0.7		Α
Protection	s (-40°C < T _j < 150°C, unless	otherwise specified)				
I _{lim}	Drain current limit	V _{IN} = 5 V; V _{DS} = 13 V	3.5	5	7	А
t _{dlim}	Step response current limit	V _{IN} = 5 V; V _{DS} = 13 V		10		μs
T _{jsh}	Over temperature shutdown		150	175	200	°C
T _{jrs}	Over temperature reset		135			°C
I _{gf}	Fault sink current	$V_{IN} = 5 \text{ V}; V_{DS} = 13 \text{ V}; T_j = T_{jsh}$	10	15	20	mA
E _{as}	Single pulse avalanche energy	starting T $_{\rm j}$ = 25°C; V $_{\rm DD}$ = 24 V; V $_{\rm IN}$ = 5 V; R $_{\rm gen}$ = R $_{\rm IN~MIN}$ = 220 Ω ; L = 24 mH (see <i>Figure 6</i> and <i>Figure 8</i>)	100			mJ

^{1.} Pulsed: Pulse duration = 300 μ s, duty cycle 1.5 %

3 Protection features

During normal operation, the input pin is electrically connected to the gate of the internal Power MOSFET through a low impedance path.

The device then behaves like a standard Power MOSFET and can be used as a switch from DC up to 50 kHz. The only difference from the user's standpoint is that a small DC current I_{ISS} (typ. 100 μ A) flows into the input pin in order to supply the internal circuitry.

The device integrates:

- Overvoltage clamp protection: internally set at 45 V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.
- Linear current limiter circuit: limits the drain current I_D to I_{lim} whatever the input pin voltages. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the over temperature threshold T_{ish}.
- Overtemperature and short circuit protection: these are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Overtemperature cutout occurs in the range 150°C to 190°C, a typical value being 170°C. The device is automatically restarted when the chip temperature falls of about 15°C below shutdown temperature.
- Status feedback: in the case of an overtemperature fault condition (T_j > T_{jsh}), the device tries to sink a diagnostic current I_{gf} through the input pin in order to indicate fault condition. If driven from a low impedance source, this current may be used in order to warn the control circuit of a device shutdown. If the drive impedance is high enough so that the input pin driver is not able to supply the current I_{gf}, the input pin will fall to 0 V. This will not however affect the device operation: no requirement is put on the current capability of the input pin driver except to be able to supply the normal operation drive current I_{ISS}.

Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL logic circuit.

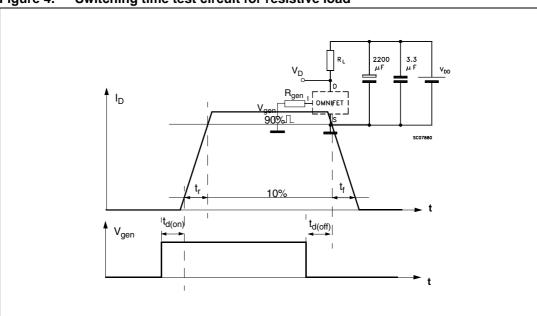


Figure 4. Switching time test circuit for resistive load

Figure 5. Test circuit for diode recovery times

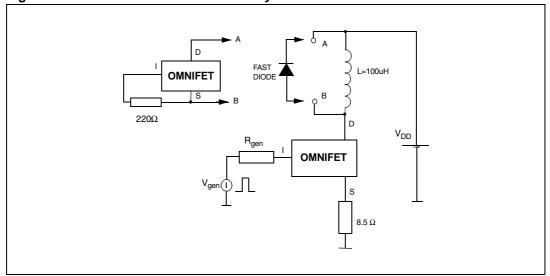


Figure 6. Unclamped inductive load test circuits

Figure 7. Input charge test circuit

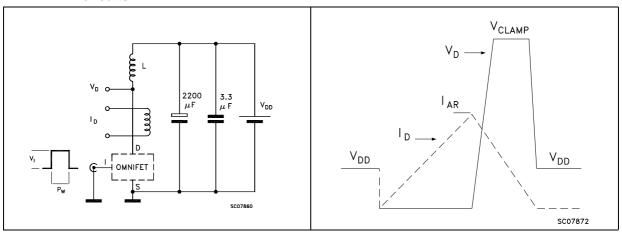
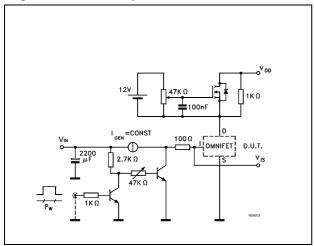
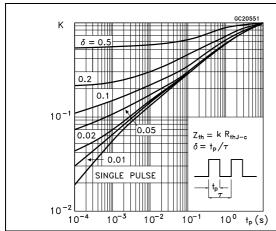


Figure 8. Unclamped inductive waveforms



3.1 Electrical characteristics curves

Figure 9. Thermal impedance for SOT-223 Figure 10. Derating curve



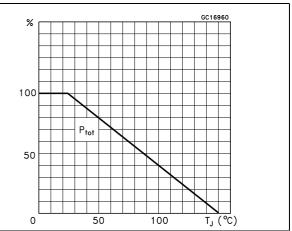
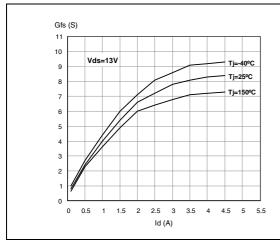


Figure 11. Transconductance

Figure 12. Static drain-source on resistance vs input voltage (part 1/2)



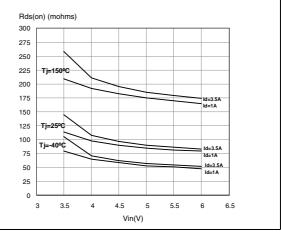
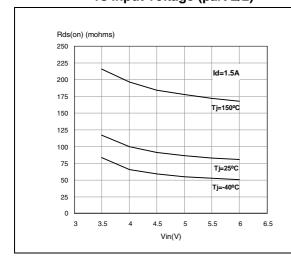
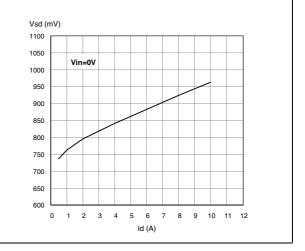


Figure 13. Static drain-source on resistance vs input voltage (part 2/2)

Figure 14. Source-drain diode forward characteristics

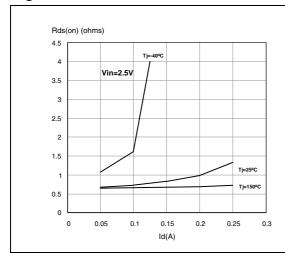




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Figure 15. Static drain source on resistance

Figure 16. Turn-on current slope (part 1/2)



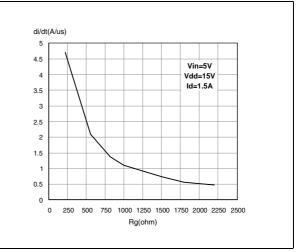
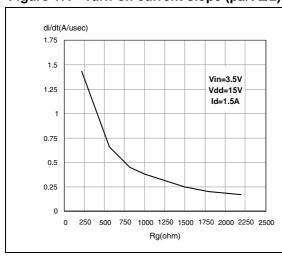


Figure 17. Turn-on current slope (part 2/2)

Figure 18. Transfer characteristics



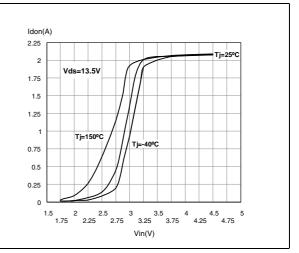
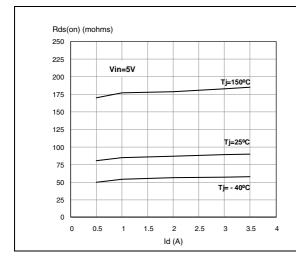
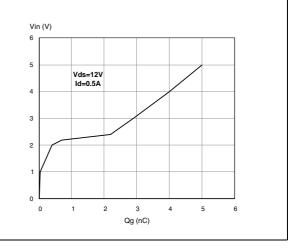


Figure 19. Static drain-source on resistance vs Id

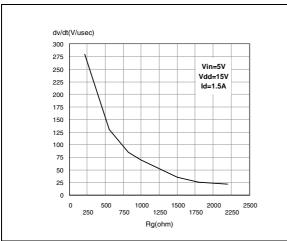
Figure 20. Input voltage vs input charge





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Figure 21. Turn-off drain source voltage slope Figure 22. Turn-off drain source voltage slope (part 1/2) (part 2/2)



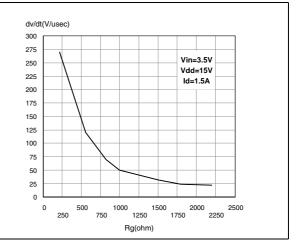
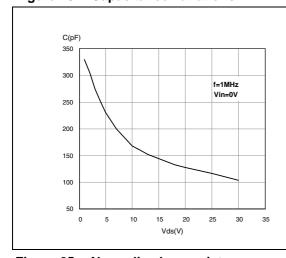


Figure 23. Capacitance variations

Figure 24. Output characteristics



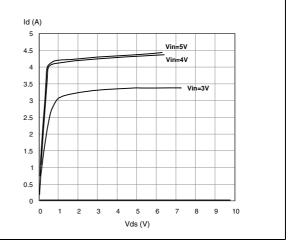
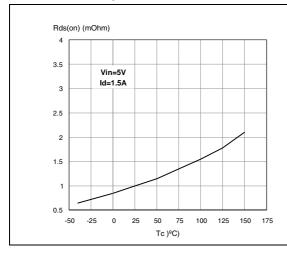
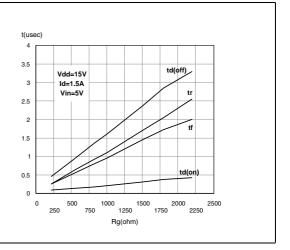


Figure 25. Normalized on resistance vs temperature

Figure 26. Switching time resistive load (part 1/2)





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Figure 27. Switching time resistive load (part 2/2)

Figure 28. Normalized input threshold voltage vs temperature

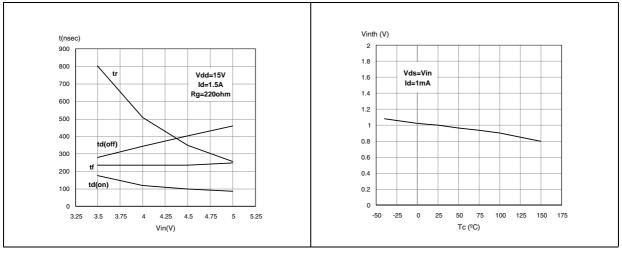
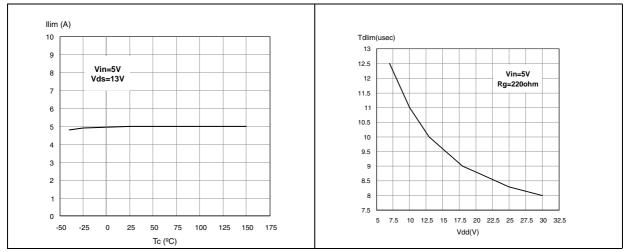


Figure 29. Normalized current limit vs junction Figure 30. Step response current limit temperature



4 Package and packing information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: <u>www.st.com</u>.

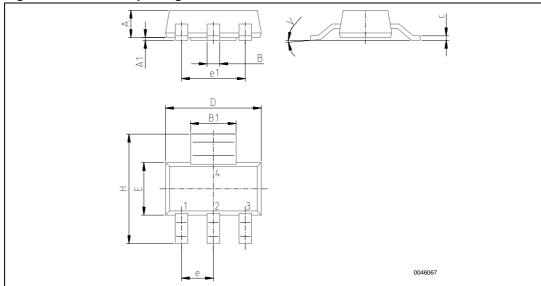
ECOPACK® is an ST trademark.

4.1 SOT-223 mechanical data

Table 5. SOT-223 mechanical data

Symbol	Millimeters			
Symbol	Min.	Тур.	Max.	
А			1.8	
В	0.6	0.7	0.85	
B1	2.9	3	3.15	
С	0.24	0.26	0.35	
D	6.3	6.5	6.7	
е		2.3		
e1		4.6		
E	3.3	3.5	3.7	
Н	6.7	7	7.3	
V		10 (max)		
A1	0.02		0.1	

Figure 31. SOT-223 package dimensions



4.2 SO-8 mechanical data

Table 6. SO-8 mechanical data

Oh		Millimeters	
Symbol	Min	Тур	Мах
Α			1.75
a1	0.1		0.25
a2			1.65
a3	0.65		0.85
b	0.35		0.48
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
С	0.17		0.23
D ⁽¹⁾	4.80	4.90	5.00
E	5.80	6.00	6.20
E1 ⁽²⁾	3.80	3.90	4.00
е		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm in total (both side).

^{2.} Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.

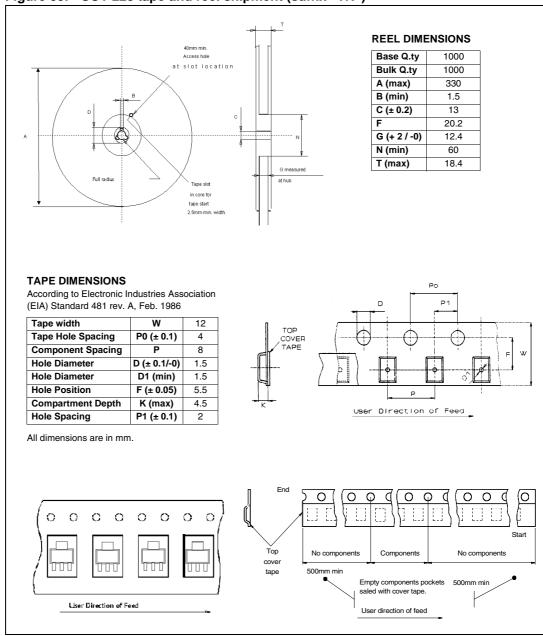
SEATING PLANE

OU16023 D

Figure 32. SO-8 package dimensions

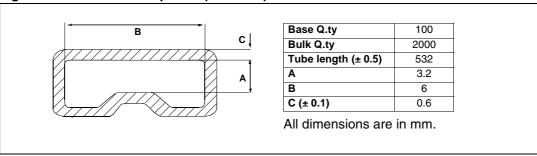
4.3 SOT-223 packing information

Figure 33. SOT-223 tape and reel shipment (suffix "TR")

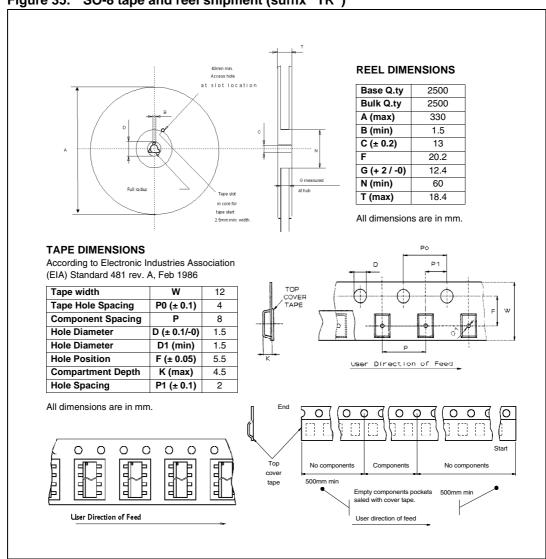


SO-8 packing information 4.4

Figure 34. SO-8 tube shipment (no suffix)



SO-8 tape and reel shipment (suffix "TR")



5 Revision history

Table 7. Document revision history

Date	Revision	Changes
24-May-2009	1	Initial release.
21-Jul-2009	2	Updated Table 1: Device summary.
29-Sep_2009	3	Removed target specification on cover page.
10-May-2012	4	Updated <i>Table 1: Device summary Table 2: Absolute maximum ratings</i> : - R _{IN MIN} : changed unit to Ω (it was W)

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